CLAIMS

What is claimed is:

1. A distributed buffering system comprises:

input buffer operably coupled to store at least one data block;

serializing module operably coupled to the input buffer, wherein the serializing module serializes at least a portion of a data block of the at least one data block when the at least a portion of the data block is read from the input buffer to produce a serial stream of data;

at least one deserializing module;

at least one output buffer; and

programmable logic device operably coupled to distribute the serial stream of data to the at least one output buffer via the at least one deserializing module based on a distribution instruction, wherein the at least one deserializing module converts the serial stream of data back into the at least a portion of the data block to produce recaptured data, and wherein the at least one output buffer stores the recaptured data.

2. The distributed buffering system of claim 1 further comprises:

memory control module operably coupled to the input buffer, the programmable logic device, and the at least one output buffer, wherein the memory control module generates a read instruction and generates a write instruction based on the distribution instruction, wherein the read instruction is provided to the input buffer and the write instruction is provided to the at least one output buffer.

3. The distributed buffering system of claim 2 further comprises:

programmable gate array programmed to function as the memory control module and to function as the programmable

logic device for distributing the serial stream of data.

4. The distributed buffering system of claim 1 further comprises:

an input integrated circuit that includes the input buffer and the serializing module; and

a plurality of output integrated circuits, wherein each of the plurality of output integrated circuits includes an output buffer and a corresponding deserializing module.

5. The distributed buffering system of claim 1, wherein the at least one output buffer includes a plurality of output buffers, wherein the at least one deserializing module includes a plurality of deserializing modules, and wherein the programmable logic device further comprises:

input interface operably coupled to receive the serial stream of data;

plurality of output interfaces operably coupled to the plurality of output buffers; and

programmable logic fabric operable to provide selective connectivity between the input interface and the plurality of output interfaces, wherein the input interface deserializes the serial stream of data to produce deserialized data and wherein each of the plurality of output interfaces selectively connected to the input interface serializes the deserialized data to recapture the serial stream of data.

6. The distributed buffering system of claim 1 further comprises:

a plurality of input buffers that include the input buffer;

a plurality of serializing modules that include the serializing module, wherein the plurality of serializing modules is operably coupled to the plurality of input buffers.

7. The distributed buffering system of claim 1, wherein the serializing module further comprises:

rate adjusting module that establishes bit rate of the serializing module based on rate of the input buffer and data width of the input buffer.

8. The distributing buffering system of claim 7, wherein the at least one output buffers further comprise:

rate adjusting module that establishes bit rate of the at least one output buffer based on the rate of the input buffer and the data width of the input buffer.

9. The distributed buffering system of claim 7, wherein the at least one output buffer further comprise:

rate adjusting module that establishes bit rate of the at least one output buffer based on rate of the at least one output buffer and data width of the at least one output buffer.

10. The distributed buffering system of claim 1, wherein the programmable logic device further comprises:

command module operably coupled to receive a buffering instruction, wherein the command module generates the distribution instruction and a logic configuration signal based on the buffering instruction, wherein the logic configuration signal configures logic of the programmable logic device.

11. The distributed buffering system of claim 1, wherein the programmable logic device further comprises:

clock module operably coupled to generate clocking signals, wherein the clock module provides the clocking signals to the input buffer, the serializing module, the plurality of deserializing modules, and the plurality of output buffers.

12. The distributed buffering system of claim 1, wherein the serializing module further comprises:

addressing module operably coupled to serialize, as part of the serial stream of data, at least one address of the at least one of the plurality of output buffers based on a buffering instruction, and wherein the programmable logic device includes an interpreting module to extract the at least one address from the serial stream of data.

13. The distributed buffering system of claim 1, wherein the programmable logic device further comprises:

memory operably coupled to buffer the serial stream of data, to delay providing of the serial stream of data to the at least one output buffer, or to cache the serial stream of data for the at least one output buffer.

14. The distributed buffering system of claim 1, wherein the input buffer further comprises:

a plurality of memories operably coupled to the serializing module, wherein each of the plurality of memories stores a corresponding portion of the at least one data block.

15. A distributed buffering system comprises:

input buffer that includes a plurality of input memories, wherein the input buffer stores at least one data block and wherein each of the plurality of input memories stores a corresponding portion of the at least one data block;

plurality of serializing modules operably coupled to the plurality of input memories, wherein each of the plurality of serializing modules serializes the corresponding portion of the at least one data block to produce a plurality of streams of data;

programmable logic device operably coupled to distribute the plurality of streams of data to at least one of a plurality of output buffers based on a distribute

instruction, wherein each of the plurality of output buffers includes a plurality of output memories; and

plurality of deserializing modules, wherein each of the plurality of deserializing modules is operably coupled to a corresponding one of the plurality of output memories of each of the plurality of output buffers, wherein corresponding ones of the plurality of deserializing modules deserializes a corresponding one of the plurality of streams of data to recapture the corresponding portions of the at least one block of data, wherein the plurality of output memories of the at least one of the output buffers stores the recaptured corresponding portions of the at least one block data.

16. The distributed buffering system of claim 15 further comprises:

controller operably coupled to the input buffer, the programmable logic, and the plurality of output buffers, wherein the controller generates the distribute instruction, generates a plurality of read instructions, and a plurality of write instructions, wherein the plurality of read instructions are provided to the plurality of input memories, and wherein the plurality of write instructions are provided to the plurality of output memories of the at least one of the plurality of output buffers.

17. The distributed buffering system of claim 16, wherein the controller further comprises:

aligning module operably coupled to align access to the recaptured corresponding portions of the at least one data block from the plurality of output memories of the at least one of the plurality of output buffers.

18. The distributed buffering system of claim 17, wherein the controller further comprises:

propagation module operably coupled to maintain propagation delay information for each path between the programmable logic device and the plurality of input memories

and for each path between the programmable logic device and the plurality of output memories of the each of the plurality of output buffers.

19. The distributed buffering system of claim 18, wherein the controller further comprises:

training module operably coupled to provide test data over each of the paths between the programmable logic device and the plurality of input memories and over each of the paths between the programmable logic device and the plurality of output memories of the each of the plurality of output buffers, wherein the propagation module determines the propagation delay information based on the test data.

20. The distributed buffering system of claim 18, wherein the programmable logic device further comprises:

memory operably coupled to provide buffering for at least some of the paths between the programmable logic device and the plurality of input memories and the paths between the programmable logic device and the plurality of output memories of the each of the plurality of output buffers to facilitate the align access to the recaptured corresponding portions of the at least one data block.

21. The distributed buffering system of claim 16, wherein the controller further comprises:

instruction buffer operably coupled to queue incoming instructions based on propagation delay of distributing the at least one data block between the input buffer and the at least one of the plurality output buffers.

22. The distributed buffering system of claim 16, wherein the controller further comprises:

synchronizing module operably coupled to synchronize distributing the at least one data block between the input buffer and the at least one of the plurality of output buffers.

23. A method for controlling a distributed buffering system, the method comprises:

receiving a buffering instruction;

interpreting the buffering instruction to identify a data block stored in an input buffer and to identify at least one targeted output buffer of a plurality of output buffers;

generating a configuration instruction to facilitate conveyance of the data block from the input buffer to the at least one targeted output buffer;

generating a read instruction and a write instruction based on the buffering instruction;

determining serialized propagation delay information for the conveyance of the data block from the input buffer to the at least one targeted output buffer;

issuing the configuration instruction to a programmable logic device;

issuing the read instruction to the input buffer such that the data block is read from the input buffer; and

issuing the write instruction to the at least one targeted output buffer subsequent to the issuing of the read instruction based on serialized propagation delay information.

24. The method of claim 23, wherein the determining the serialized propagation delay information further comprises:

accessing segment propagation delay information relating to propagation delay between the input buffer and the programmable logic device and between each of the plurality of output buffers and the programmable logic device; and

establishing the propagation delay information based on the segment propagation delay information between the input buffer and the programmable logic device and the at least one targeted output buffer and the programmable logic device.

25. The method of claim 24 further comprises:

initiating transference of test data between the input buffer and the programmable logic device;

determining propagation delay for the transference of the test data between the input buffer and the programmable logic device;

initiating transference of the test data between the programmable logic device and each of the plurality of output buffer;

determining propagation delay for the transference of the test data between the programmable logic device and the each of the plurality of output buffers; and

tabulating the propagation delays for the transference of the test data between the programmable logic device and the input buffer and the plurality of output buffers to produce the propagation delay information.

26. The method of claim 23 further comprises:

determining a serializing rate for serializing the data block for conveyance from the input buffer to the programmable logic device based on rate of the input buffer and data width of the input buffer.

27. The method of claim 23 further comprises:

determining a serializing rate for conveyance of a serialized representation of the data block from the programmable logic device to the at least one targeted output buffer based on rate of the at least one targeted output buffer and data width of the at least one targeted output buffer.

28. The method of claim 27 further comprises:

aligning processing of subsequent buffering instructions based on the serializing rate.

29. An apparatus for controlling a distributed buffering system, the apparatus comprises:

processing module; and

memory operably coupled to the processing module, wherein the memory includes operational instructions that cause the processing module to:

receive a buffering instruction;

interpret the buffering instruction to identify a data block stored in an input buffer and to identify at least one targeted output buffer of a plurality of output buffers;

generate a configuration instruction to facilitate conveyance of the data block from the input buffer to the at least one targeted output buffer;

generate a read instruction and a write instruction based on the buffering instruction;

determine serialized propagation delay information for the conveyance of the data block from the input buffer to the at least one targeted output buffer;

issue the configuration instruction to a programmable logic device;

issue the read instruction to the input buffer such that the data block is read from the input buffer; and

issue the write instruction to the at least one targeted output buffer subsequent to the issuing of the read instruction based on serialized propagation delay information.

30. The apparatus of claim 29, wherein the memory further comprises operational instructions that cause the processing module to determine the serialized propagation delay information by:

accessing segment propagation delay information relating to propagation delay between the input buffer and the programmable logic device and between each of the plurality of output buffers and the programmable logic device; and

establishing the propagation delay information based on the segment propagation delay information between the input buffer and the programmable logic device and the at least one targeted output buffer and the programmable logic device.

31. The apparatus of claim 30, wherein the memory further comprises operational instructions that cause the processing module to:

initiate transference of test data between the input buffer and the programmable logic device;

determine propagation delay for the transference of the test data between the input buffer and the programmable logic device;

initiate transference of the test data between the programmable logic device and each of the plurality of output buffer;

determine propagation delay for the transference of the test data between the programmable logic device and the each of the plurality of output buffers; and

tabulate the propagation delays for the transference of the test data between the programmable logic device and the input buffer and the plurality of output buffers to produce the propagation delay information.

32. The apparatus of claim 29, wherein the memory further comprises operational instructions that cause the processing module to:

determine a serializing rate for serializing the data block for conveyance from the input buffer to the programmable logic device based on rate of the input buffer and data width of the input buffer.

33. The apparatus of claim 29, wherein the memory further comprises operational instructions that cause the processing module to:

determine a serializing rate for conveyance of a serialized representation of the data block from the programmable logic device to the at least one targeted output buffer based on rate of the at least one targeted output buffer and data width of the at least one targeted output buffer.

34. The apparatus of claim 33, wherein the memory further comprises operational instructions that cause the processing module to:

align processing of subsequent buffering instructions based on the serializing rate.

35. A network component comprises:

network data processing module operably coupled to perform a network function upon ingress network data to produce egress network data, wherein the network processing module generates a distribution instruction based on the network function;

input buffer operably coupled to store at least one data block of the egress network data;

serializing module operably coupled to the input buffer, wherein the serializing module serializes at least a portion of a data block of the at least one data block when the at least a portion of the data block is read from the input buffer to produce a serial stream of data;

at least one deserializing module;

at least one output buffer; and

programmable logic device operably coupled to distribute the serial stream of data to the at least one output buffer via the at least one deserializing module based on a distribution instruction, wherein the at least one deserializing module converts the serial stream of data back into the at least a portion of the data block to produce recaptured data, and wherein the at least one output buffer stores the recaptured data.

36. The network component of claim 35 further comprises:

memory control module operably coupled to the input buffer, the programmable logic device, and the at least one output buffer, wherein the memory control module generates a read instruction, and generates a write instruction, wherein the read instruction is provided to the input buffer and the

write instruction is provided to the at least one output buffer.

37. The network component of claim 35, wherein the programmable logic device further comprises:

input interface operably coupled to receive the serial stream of data;

at least one output interface operably coupled to the at least one output buffer; and

programmable logic fabric operable to provide selective connectivity between the input interface and the at least one output interface, wherein the input interface deserializes the serial stream of data and wherein the at least one output interface serializes data recapture the serial stream of data.

38. The network component of claim 35 further comprises:

a plurality of input buffers that include the input buffer;

a plurality of serializing modules that include the serializing module, wherein the plurality of serializing modules is operably coupled to the plurality of input buffers.

39. The network component of claim 35, wherein the serializing module further comprises:

rate adjusting module that establishes bit rate of the serializing module based on rate of the input buffer and data width of the input buffer.

40. The network component of claim 39, wherein the at least one output buffer further comprise:

rate adjusting module that establishes bit rate of the at least one output buffer based on the rate of the input buffer and the data width of the input buffer.

41. The network component of claim 39, wherein the at least one output buffer further comprise:

rate adjusting module that establishes bit rate of the at least one output buffer based on rate of the at least one output buffer and data width of the at least one output buffer.

42. The network component of claim 35, wherein the network data processing module further comprises:

command module operably coupled to generate the distribution instruction, a read command, and a write command based on a buffering instruction associated with the network function.

43. The network component of claim 35, wherein the serializing module further comprises:

addressing module operably coupled to serialize, as part of the serial stream of data, at least one address of the at least one of the plurality of output buffers based on a buffering instruction, and wherein the programmable logic device includes an interpreting module to extract the at least one address from the serial stream of data.

44. The network component of claim 35, wherein the programmable logic device further comprises:

memory operably coupled to buffer the serial stream of data to delay providing of the serial stream of data to the at least one output buffer, or to cache the serial stream of data for the at least one output buffer.

45. The network component of claim 35, wherein the input buffer further comprises:

a plurality of memories operably coupled to the serializing module, wherein each of the plurality of memories stores a corresponding portion of the at least one data block.

46. A network component comprises:

input buffer operably coupled to store at least one data block of ingress network data;

serializing module operably coupled to the input buffer, wherein the serializing module serializes at least a portion of a data block of the at least one data block when the at least a portion of the data block is read from the input buffer to produce serial ingress network data;

network data processing module operably coupled to perform a network function upon the serial ingress network data to produce serial egress network data, wherein the network processing module generates a distribution instruction based on the network function;

plurality of deserializing modules operably coupled to the network data processing module, wherein at least one of the plurality of deserializing modules, based on the distribution instruction, converts the serial egress network data into data blocks of egress network data; and

a plurality of output buffers operably coupled to the plurality of deserializing modules, wherein at least one of the plurality of output buffers associated with the at least one of the plurality of deserializing modules, based on the distribution instruction, stores at least one of the data blocks of the egress network data.

47. The network component of claim 46 further comprises:

memory control module operably coupled to the input buffer, the network data processing module, and the plurality of output buffers, wherein the generates a read instruction, and generates a write instruction, wherein the read instruction is provided to the input buffer and the write instruction is provided to the at least one of the plurality of output buffers.

48. The network component of claim 46, wherein the network data processing module further comprises:

input interface operably coupled to receive the serial

stream of data;

plurality of output interfaces operably coupled to the plurality of output buffers; and

programmable logic fabric operable to provide selective connectivity between the input interface and the plurality of output interfaces and to perform at least a portion of the network function, wherein the input interface deserializes the serial stream of data and wherein each of the plurality of output interfaces serializes data recapture the serial stream of data.

49. The network component of claim 46, wherein the serializing module further comprises:

rate adjusting module that establishes bit rate of the serializing module based on rate of the input buffer and data width of the input buffer.

50. The network component of claim 49, wherein each of the plurality of output buffers further comprise:

rate adjusting module that establishes bit rate of the each of the plurality of output buffers based on the rate of the input buffer and the data width of the input buffer.

51. The network component of claim 49, wherein each of the plurality of output buffers further comprise:

rate adjusting module that establishes bit rate of each of the plurality of output buffers based on rate of the each of the plurality of output buffers and data width of each of the plurality of output buffers.

52. The network component of claim 46, wherein the serializing module further comprises:

addressing module operably coupled to serialize, as part of the serial stream of data, at least one address of the at least one of the plurality of output buffers based on a buffering instruction, and wherein the programmable logic device includes an interpreting module to extract the at

least one address from the serial stream of data.

53. The network component of claim 46, wherein the network data processing module further comprises:

memory operably coupled to buffer the serial stream of data to delay providing of the serial stream of data to the at least one of the plurality of output buffers, or to cache the serial stream of data for the at least one of the plurality of output buffers.

54. The network component of claim 46, wherein the input buffer further comprises:

a plurality of memories operably coupled to the serializing module, wherein each of the plurality of memories stores a corresponding portion of the at least one data block.

55. A network component comprises:

input buffer that includes a plurality of input memories, wherein the input buffer stores at least one data block and wherein each of the plurality of input memories stores a corresponding portion of the at least one data block;

plurality of serializing modules operably coupled to the plurality of input memories, wherein each of the plurality of serializing modules serializes the corresponding portion of the at least one data block to produce a plurality of streams of data;

plurality of output buffers, wherein each of the plurality of output buffers includes a plurality of output memories;

plurality of deserializing modules, wherein each of the plurality of deserializing modules is operably coupled to a corresponding one of the plurality of output memories of each of the plurality of output buffers; and

network data processing module operably coupled to perform a network function upon the plurality of streams of

data to produce processed streams of data and to distribute the processed streams of data to the plurality of output memories of at least one of a plurality of output buffers via the corresponding ones of the plurality of deserializing modules based on the network function, wherein the corresponding ones of the plurality of deserializing modules deserializes a corresponding one of the plurality of streams of data to recapture the corresponding portions of the at least one block of data, wherein the plurality of output memories of the at least one of the output buffers stores the recaptured corresponding portions of the at least one block data.

56. The network component of claim 55, wherein the network data processing module further comprises:

controller operably coupled to the input buffer, the programmable logic, and the plurality of output buffers, wherein the controller generates a plurality of read instructions and a plurality of write instructions in accordance with the network function, wherein the plurality of read instructions are provided to the plurality of input memories, and wherein the plurality of write instructions are provided to the plurality of output memories of the at least one of the plurality of output buffers.

57. The network component of claim 56, wherein the controller further comprises:

aligning module operably coupled to align access to the recaptured corresponding portions of the at least one data block from the plurality of output memories of the at least one of the plurality of output buffers.

58. The network component of claim 57, wherein the controller further comprises:

propagation module operably coupled to maintain propagation delay information for each path between the programmable logic device and the plurality of input memories

and for each path between the programmable logic device and the plurality of output memories of the each of the plurality of output buffers.

59. The network component of claim 58, wherein the controller further comprises:

training module operably coupled to provide test data over each of the paths between the programmable logic device and the plurality of input memories and over each of the paths between the programmable logic device and the plurality of output memories of the each of the plurality of output buffers, wherein the propagation module determines the propagation delay information based on the test data.

60. The network component of claim 58, wherein the network data processing module further comprises:

memory operably coupled to provide buffering for at least some of the paths between the programmable logic device and the plurality of input memories and the paths between the programmable logic device and the plurality of output memories of the each of the plurality of output buffers to facilitate the align access to the recaptured corresponding portions of the at least one data block.

61. The network component of claim 56, wherein the controller further comprises:

instruction buffer operably coupled to queue incoming instructions based on propagation delay of distributing the at least one data block between the input buffer and the at least one of the plurality output buffers.

62. The network component of claim 56, wherein the controller further comprises:

synchronizing module operably coupled to synchronize distributing the at least one data block between the input buffer and the at least one of the plurality of output buffers.

63. A buffering system comprises:

programmable logic device that processes data while performing a function;

memory for storing the data;

deserializing module operably coupled to receive a serial stream of the data from the programmable logic device and to convert the serial stream of the data into words of the data, wherein the deserializing module provides the words of the data to the memory for storage; and

serializing module operably coupled to receive the stored words of the data from the memory and to convert the stored words of the data into serial data to produce a recaptured serial stream of the data, wherein the serializing module provides the recaptured serial stream of the data to the programmable logic device.

64. The buffering system of claim 63, further comprises:

memory control module operably coupled to the memory and the programmable logic device, wherein the memory control module generates a read instruction and generates a write instruction for reading and writing the words of the data into and from the memory.

65. The buffering system of claim 64 further comprises:

programmable gate array programmed to function as the memory control module and to function as the programmable logic device.

66. The buffering system of claim 63, wherein the programmable logic device further comprises:

input interface operably coupled to receive the recaptured serial stream of data;

output interface operably coupled to provide the serial stream of the data; and

programmable logic fabric operably configured to perform the function.

67. The buffering system of claim 63, wherein the serializing module further comprises:

rate adjusting module that establishes bit rate of the serializing module based on rate of the memory and data width of the memory.

68. The buffering system of claim 63, wherein the programmable logic device further comprises:

clock module operably coupled to generate clocking signals, wherein the clock module provides the clocking signals to the memory, the serializing module, and the deserializing module.

69. The buffering system of claim 63, wherein the programmable logic device further comprises:

memory operably coupled to buffer the serial stream of data, or to delay providing of the serial stream of data to the deserializing module.